

What Is Claimed Is:

- 1 1. A method for designing an integrated circuit using a mask-
2 programmable fabric, which contains both mask-programmable logic and a mask-
3 programmable interconnect, the method comprising:
4 receiving a description of a mask-programmable cell, wherein instances of
5 the mask-programmable cell are repeated to form the mask-programmable fabric;
6 using the description of the mask-programmable cell to generate a derived
7 library containing cells that can be obtained by programming the mask-
8 programmable cell;
9 receiving a high-level design for the integrated circuit;
10 performing a synthesis operation on the high-level design to generate a
11 preliminary netlist for the high-level design that contains references to cells in the
12 derived library; and
13 converting the preliminary netlist into a netlist that contains references to
14 the mask-programmable cell.
- 1 2. The method of claim 1, further comprising performing a placement
2 operation and a routing operation on the netlist to produce a layout for the
3 integrated circuit.
- 1 3. The method of claim 2, wherein performing the routing operation
2 involves programming the mask-programmable logic and mask-programmable
3 interconnect.

1 4. The method of claim 1, wherein the mask-programmable logic and
2 the mask-programmable interconnect that make up the mask-programmable fabric
3 can be programmed by changing inter-metal via layers and/or metal layers

1 5. The method of claim 1, wherein the method further comprises
2 performing a packing operation on the netlist to combine cells that can use free
3 resources from other cells.

1 6. The method of claim 5, wherein performing the packing operation
2 involves considering:
3 drive strengths of output pins for mask-programmable cells;
4 routability of pins for mask-programmable cells;
5 net count for mask-programmable cells; and
6 active pin count for mask-programmable cells.

1 7. The method of claim 1, wherein the mask-programmable cell
2 includes a sequential logic portion, and wherein the derived library contains a
3 sequential cell, which corresponds the sequential logic portion of the mask-
4 programmable cell.

1 8. The method of claim 1,
2 wherein the description of the mask-programmable cell defines one or
3 more pins;
4 wherein a pin may be specified as being tied to, power, ground, a route
5 segment or another pin;
6 wherein a pin may be associated with a logic function; and
7 wherein a pin may be specified as part of a sequential element.

1 9. The method of claim 8,
2 wherein the description of the mask-programmable cell defines route
3 segments for routing signals within the mask-programmable fabric;
4 wherein route segments may be horizontal, vertical or at any angle;
5 wherein several route segments may be collinear; and
6 wherein route segments may be coupled to pins or to other route segments.

1 10. The method of claim 9,
2 wherein the description of the mask-programmable fabric includes
3 information related to timing for route segments and connections; and
4 wherein the information related to timing can be used while performing a
5 routing operation for the mask-programmable fabric.

1 11. A computer-readable storage medium storing instructions that
2 when executed by a computer cause the computer to perform a method for
3 designing an integrated circuit using a mask-programmable fabric, which contains
4 both mask-programmable logic and a mask-programmable interconnect, the
5 method comprising:
6 receiving a description of a mask-programmable cell, wherein instances of
7 the mask-programmable cell are repeated to form the mask-programmable fabric;
8 using the description of the mask-programmable cell to generate a derived
9 library containing cells that can be obtained by programming the mask-
10 programmable cell;
11 receiving a high-level design for the integrated circuit;

12 performing a synthesis operation on the high-level design to generate a
13 preliminary netlist for the high-level design that contains references to cells in the
14 derived library; and
15 converting the preliminary netlist into a netlist that contains references to
16 the mask-programmable cell.

1 12. The computer-readable storage medium of claim 11, wherein the
2 method further comprises performing a placement operation and a routing
3 operation on the netlist to produce a layout for the integrated circuit.

1 13. The computer-readable storage medium of claim 12, wherein
2 performing the routing operation involves programming the mask-programmable
3 logic and mask programmable interconnect.

1 14. The computer-readable storage medium of claim 11, wherein the
2 mask-programmable logic and the mask-programmable interconnect that make up
3 the mask-programmable fabric can be programmed by changing inter-metal via
4 layers and/or metal layers.

1 15. The computer-readable storage medium of claim 11, wherein the
2 method further comprises performing a packing operation on the netlist to
3 combine cells that can use free resources from other cells.

1 16. The computer-readable storage medium of claim 15, wherein
2 performing the packing operation involves considering:
3 drive strengths of output pins for mask-programmable cells;
4 routability of pins for mask-programmable cells;

5 net count for mask-programmable cells; and
6 active pin count for mask-programmable cells.

1 17. The computer-readable storage medium of claim 11, wherein the
2 mask-programmable cell includes a sequential logic portion, and wherein the
3 derived library contains a sequential cell, which corresponds the sequential logic
4 portion of the mask-programmable cell.

1 18. The computer-readable storage medium of claim 11,
2 wherein the description of the mask-programmable cell defines one or
3 more pins;
4 wherein a pin may be specified as being tied to, power, ground, a route
5 segment or another pin;
6 wherein a pin may be associated with a logic function; and
7 wherein a pin may be specified as part of a sequential element.

1 19. The computer-readable storage medium of claim 18,
2 wherein the description of the mask-programmable cell defines route
3 segments for routing signals within the mask-programmable fabric;
4 wherein route segments may be horizontal, vertical or at any angle;
5 wherein several route segments may be collinear; and
6 wherein route segments may be coupled to pins or to other route segments.

1 20. The computer-readable storage medium of claim 19,
2 wherein the description of the mask-programmable fabric includes
3 information related to timing for route segments and connections; and

4 wherein the information related to timing can be used while performing a
5 routing operation for the mask-programmable fabric.

1 21. An apparatus that facilitates designing an integrated circuit using a
2 mask-programmable fabric, which contains both mask-programmable logic and a
3 mask-programmable interconnect, the apparatus comprising:

4 a receiving mechanism configured to receive a description of a mask-
5 programmable cell, wherein instances of the mask-programmable cell are repeated
6 to form the mask-programmable fabric;

7 a deriving mechanism configured to use the description of the mask-
8 programmable cell to generate a derived library containing cells that can be
9 obtained by programming the mask-programmable cell;

10 wherein the receiving mechanism is additionally configured to receive a
11 high-level design for the integrated circuit;

12 a synthesis mechanism configured to perform a synthesis operation on the
13 high-level design to generate a preliminary netlist for the high-level design that
14 contains references to cells in the derived library; and

15 a conversion mechanism configured to convert the preliminary netlist into
16 a netlist that contains references to the mask-programmable cell.

1 22. The apparatus of claim 21, further comprising a placement
2 mechanism and a routing mechanism configured to perform a placement operation
3 and a routing operation, respectively, on the netlist to produce a layout for the
4 integrated circuit.

1 23. The apparatus of claim 22, wherein the routing mechanism is
2 configured to program the mask-programmable logic and mask programmable
3 interconnect.

1 24. The apparatus of claim 21, wherein the mask-programmable logic
2 and the mask-programmable interconnect that make up the mask-programmable
3 fabric can be programmed by changing inter-metal via layers and/or metal layers.

1 25. The apparatus of claim 21, wherein the apparatus further comprises
2 a packing mechanism configured to perform a packing operation on the netlist to
3 combine cells that can use free resources from other cells.

1 26. The apparatus of claim 25, wherein performing the packing
2 operation involves considering:
3 drive strengths of output pins for mask-programmable cells;
4 routability of pins for mask-programmable cells;
5 net count for mask-programmable cells; and
6 active pin count for mask-programmable cells.

1 27. The apparatus of claim 21, wherein the mask-programmable cell
2 includes a sequential logic portion, and wherein the derived library contains a
3 sequential cell, which corresponds to the sequential logic portion of the mask-
4 programmable cell.

1 28. The apparatus of claim 21,
2 wherein the description of the mask-programmable cell defines one or
3 more pins;

4 wherein a pin may be specified as being tied to, power, ground, a route
5 segment or another pin;

6 wherein a pin may be associated with a logic function; and

7 wherein a pin may be specified as part of a sequential element.

1 29. The apparatus of claim 28,

2 wherein the description of the mask-programmable cell defines route
3 segments for routing signals within the mask-programmable fabric;

4 wherein route segments may be horizontal, vertical or at any angle;

5 wherein several route segments may be collinear; and

6 wherein route segments may be coupled to pins or to other route segments.

1 30. The apparatus of claim 29,

2 wherein the description of the mask-programmable fabric includes
3 information related to timing for route segments and connections; and

4 wherein the information related to timing can be used while performing a
5 routing operation for the mask-programmable fabric.

1 31. An integrated circuit created through a process that uses a mask-
2 programmable fabric to design the integrated circuit, wherein the mask-
3 programmable fabric contains both mask-programmable logic and a mask-
4 programmable interconnect, the process comprising:

5 receiving a description of a mask-programmable cell, wherein instances of
6 the mask-programmable cell are repeated to form the mask-programmable fabric;

7 using the description of the mask-programmable cell to generate a derived
8 library containing cells that can be obtained by programming the mask-
9 programmable cell;

10 receiving a high-level design for the integrated circuit;
11 performing a synthesis operation on the high-level design to generate a
12 preliminary netlist for the high-level design that contains references to cells in the
13 derived library; and
14 converting the preliminary netlist into a netlist that contains references to
15 the mask-programmable cell.

1 32. A mask for use in an optical lithography process for manufacturing
2 an integrated circuit, wherein the mask is generated through a process that uses a
3 mask-programmable fabric to design the integrated circuit, wherein the mask-
4 programmable fabric contains both mask-programmable logic and a mask-
5 programmable interconnect, the process comprising:
6 receiving a description of a mask-programmable cell, wherein instances of
7 the mask-programmable cell are repeated to form the mask-programmable fabric;
8 using the description of the mask-programmable cell to generate a derived
9 library containing cells that can be obtained by programming the mask-
10 programmable cell;
11 receiving a high-level design for the integrated circuit;
12 performing a synthesis operation on the high-level design to generate a
13 preliminary netlist for the high-level design that contains references to cells in the
14 derived library; and
15 converting the preliminary netlist into a netlist that contains references to
16 the mask-programmable cell.